a) a host side memory controller region having a memory access request input and a memory command packet chunk output, a memory command packet chunk being a portion of a memory command packet, said host side memory controller region clocked by a first clock; and

b) a memory side memory controller region having a memory command packet chunk input coupled to said memory command packet chunk output, said memory side memory controller region clocked by a second clock, said second clock different than said first clock.

14. (New) The apparatus of claim 13 wherein said memory command packet chunk output further comprises a row output and a column output.

15. (New) The apparatus of claim 13 wherein said host side memory controller region further comprises a scheduler coupled to said memory access request input, said scheduler configured to generate said memory command packet.

16. (New) The apparatus of claim 15 wherein said scheduler is coupled to a queue.

17. (New) The apparatus of claim 15 wherein said memory command packet is a row command.

18. (New) The apparatus of claim 15 wherein said memory command packet is a column command.

19. (New) The apparatus of claim 15 wherein said scheduler further comprises logic to determine when resource conflicts may arise.

20. (New) The apparatus of claim 13 wherein said host side memory controller region further comprises a second memory command packet chunk output.

21. (New) The apparatus of claim 20 wherein said second clock is faster than said first clock.

22. (New) The apparatus of claim 20 wherein said host side memory controller region is configured to present a second memory command packet chunk upon said second memory command packet chunk output, said second memory command packet chunk a portion of a second memory command packet.

23. (New) An apparatus, comprising:

a) a memory controller comprising a host side region and a memory side region, said host region having a memory access request input and a memory command packet chunk output, a memory command packet chuck being a portion of a memory command packet, said host side region clocked by a first clock, said memory side region having a memory command packet chunk input coupled to said memory command packet chunk output, said memory side

region clocked by a second clock, said second clock different than said first clock; and

b) a memory coupled to said memory side region.

24. (New) The apparatus of claim 23 further comprising an external agent configured to read and write to said memory via said memory controller.

25. (New) The apparatus of claim 24 wherein said external agent further comprises a processor.

26. (New) The apparatus of claim 24 wherein said external agent further comprises a graphics subsystem.

27. The apparatus of claim 24 wherein said external agent further comprises an expansion bus master.

28. (New) The apparatus of claim 23 wherein said memory command packet chunk output further comprises a row output and a column output.

29. (New) The apparatus of claim 23 wherein said host side memory controller region further comprises a scheduler coupled to said memory access request input, said scheduler configured to generate said memory command packet.

30. (New) The apparatus of claim 29 wherein said scheduler is coupled to a queue.

31. (New) The apparatus of claim 29 wherein said memory command packet is a row command.

32. (New) The apparatus of claim 29 wherein said memory command packet is a column command.

33. (New) The apparatus of claim 29 wherein said scheduler further comprises logic to determine when resource conflicts may arise.

34. (New) The apparatus of claim 23 wherein said host side memory controller region further comprises a second memory command packet chunk output.

35. (New) The apparatus of claim 34 wherein said second clock is faster than said first clock.

36. (New) The apparatus of claim 34 wherein said host side memory controller region is configured to present a second memory command packet chunk upon said second memory command packet chunk output, said second memory command packet chunk a portion of a second memory command packet.

37. (New) A method, comprising:

a) generating a memory command packet from a memory request while clocked by a first clock; and

b) sending a memory command packet chunk to a memory controller region clocked by a second clock, a memory command packet chuck being a portion of said memory command packet, said second clock different than said first clock.

38. (New) The method of claim 37 further comprising sending a second memory command packet chunk along with said memory command packet chunk, said second memory command packet chunk associated with a subsequent memory command packet.

39. (New) The apparatus of claim 37 wherein said memory command packet further comprises a row command.

40. (New) The apparatus of claim 39 wherein said row command activates a memory row.

41. (New) The apparatus of claim 39 wherein said row command precharges a memory row.

42. (New) The apparatus of claim 39 wherein said memory command packet further comprises a column command.

43. (New) The apparatus of claim 39 wherein said column command is used to read from a memory device.

44. (New) The apparatus of claim 39 wherein said column command is used to write to a memory device.

COMMENTS

Claims 1 through 12 have been canceled without prejudice. New claims 13 through 44 have been added. Applicant respectfully requests the examination of new claims 13 through 44 and allowance of same.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 3/14, 2000

John P. Ward
Registration No. 40,216

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA. 90025-1026
(408) 720-8598